REMARKS/ARGUMENTS

Claims 1-4, 6-18, and 20-42 are pending.

Claims 1, 3, 4, 6-14, 27, and 29-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakaya (US 5,978,830) in view of Yamaura (US 6,175,890). Claims 2, 15-18, 20-26, 28, and 35-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakaya in view of Yamaura, further in view of Pierson et al. ("Context-Agile Encryption for High Speed Communication Networks"). Applicants submit that all of the claims currently pending in this application are patentably distinguishable over the cited references, and reconsideration and allowance of this application are respectfully requested.

Independent claim 1 recites "processing first data associated with an older control record in a first processing engine; enabling a first interrupt indicator in the older control record when the processing of the first data is completed; processing second data associated with a younger control record in a second processing engine; enabling a second interrupt indicator in the younger control record when the processing of the second data is completed; and moving the second interrupt indicator associated with the younger control record onto the first interrupt indicator associated with the older control record if processing of the second data completes before processing of the first data." None of the cited references, alone or in combination, teach or suggest the above limitation.

Nakaya describes a multiple parallel-job scheduling method and apparatus. However, the system of Nakaya does not enable "a first interrupt indicator in the older control record when the processing of the first data is completed," or enable "a second interrupt indicator in the younger control record when the processing of the second data is completed." Rather, Nakaya assigns a group of parallel processors to a job. When the job is completed, there is an indication that the parallel processors are now available for a second job. Nakaya does not process the second job, until the fist job is completed and the parallel processors are available.

Nakaya is very clear about this through out the specification. For example, Nakaya states that

when the first bit of the register 4110 of the synchronization range indicator 4100 is consulted, it is indicated that the bit is set with "1" and the job J10 is allowed for the parallel computation, so that a synchronization point arrival instruction SRL1 for invocation SYN1 is executed without alteration and the instructions P102 to P106 in the parallel computing part are started. On the other hand, if the job J20 executes a synchronization point arrival instruction SRL2 during the execution of the instructions P102 to P106 in the parallel computing part by the job J10 to meet an invocation SYN2 of the parallel computing part, an interrupt INT1 is generated on the processor because "0" is set to the second bit of the register 4110 of the synchronization range indicator 4100. In response to this interrupt INT1, a scheduler SCH1 is invoked, with the result that a parallel computing request REQ1 is put in a parallel execution waiting queue CUE and the assignment of parallel processors is waited for.

Col. 21, lines 5-21, emphasis added.

Furthermore, "the synchronization range indicator 4100 is used as a parallel processor affinity indicator which indicates the affinity between serial processors and parallel processors. (Col. 21, lines 62-65, emphasis added.).

In other words, for assigned processors, "start of the parallel computation is allowed without alteration but for a parallel computation request by a serial processor not assigned with parallel processors, an interrupt is generated to invoke the scheduler so as to establish a waiting state, permitting an invocation request to be put in the parallel execution waiting queue." (Col. 21, lines 48-54, emphasis added.).

Upon "the termination of the instructions P102 to P106 in the parallel computing part of the job J10, each of the parallel processors 1005 to 1008 issues a parallel computing part termination notice END1 for indicating that the parallel processors are to be transferred to the job put in the parallel execution waiting queue. In response to this termination notice END1, an interrupt INT2 is invoked on the parallel processors 1005 to 1008. (Col. 22, lines 29-36, emphasis added.).

The termination notice END1 is further defined as "a termination notice (parallel computing part termination notice) for immediately switching the assignment of the parallel processors to the execution of a parallel computing part of another job is issued. With the parallel computing part termination notice issued, an interrupt is invoked on processors constituting parallel processors." (Col. 22, lines 22-28, emphasis added.).

Therefore, there is no teaching or suggestion in Nakaya about "processing first data associated with an older control record in a first processing engine; enabling a first interrupt indicator in the older control record when the processing of the first data is completed; processing second data associated with a younger control record in a second processing engine; enabling a second interrupt indicator in the younger control record when the processing of the second data is completed," as required by claim 1.

Moreover, Nakaya does not teach or suggest "moving the second interrupt indicator associated with the younger control record onto the first interrupt indicator associated with the older control record if processing of the second data completes before processing of the first data." First, as the Examiner acknowledges Nakaya does not disclose the enablement of a first interrupt in the older control record or the enablement of a second interrupt in the younger control record. Second, Nakaya does not disclose "moving the second interrupt indicator . . . onto the first interrupt indicator."

Yamaura does not cure the above-mentioned deficiencies of Nakaya. Even assuming arguendo that Yamaura discloses the enablement of a first interrupt in the older control record or the enablement of a second interrupt in the younger control record, it alone or in combination with Nakaya, does not teach or suggest, "processing first data associated with an older control record in a first processing engine; enabling a first interrupt indicator in the older control record when the processing of the first data is completed; processing second data associated with a younger control record in a second processing engine; enabling a second interrupt indicator in the younger control record when the processing of the second data is completed; and moving the second interrupt indicator associated with the younger control record onto the first interrupt

indicator associated with the older control record if processing of the second data completes before processing of the first data," as recited by the independent claim 1.

As a result, the combination of Nakaya and Yamaura does not teach or suggest all of the limitations of claim 1. Consequently claim 1 is patentable in view of the cited references.

Independent claim 15 includes a similar limitation of "wherein the history buffer is configured to move the first interrupt indicator associated with the first control record onto a second interrupt indicator associated with the second control record if processing of the first control record completes before processing of the second control record." Therefore, claim 15 is also patentable in view of Nakaya and Yamaura combination for the same reasons discussed above.

In summary, independent claims 1, 15, 27, and 35 define a novel and unobvious invention over the cited references. Dependent claims 2-4, 6-14, 16-18, 20-26, 28-34, and 36-42 are dependent from claims 1, 15, 27 and 35, respectively and therefore include all the limitations of their respective independent claims and additional limitations therein. Accordingly, these claims are also allowable over the cited references, as being dependent from allowable independent claims and for the additional limitations they include therein.

In view of the foregoing remarks, it is respectfully submitted that this application is now in condition for allowance, and accordingly, reconsideration and allowance are respectfully requested.

Respectfully submitted,
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